Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **1 N. CLR**
2. **1D**
3. **1CLK**
4. **1 N. PRE**
5. **1Q**
6. **1 N.Q**
7. **GND**
8. **2 N.Q**
9. **2 Q**
10. **2 N.PRE**
11. **2 CLK**
12. **2 D**
13. **2 N. CLR**
14. **VCC**

**.055”**

**.048”**

**2 1 14 13**

**6 7 8 9**

**3**

**4**

**5**

**12**

**11**

**10**

**MASK**

**REF**

**ACT74**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential:**

**Mask Ref: ACT74**

**APPROVED BY: DK DIE SIZE .048” X .055” DATE: 5/6/19**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: 54ACT74**

**DG 10.1.2**

#### Rev B, 7/1